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Dr. William Ellersick

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Education

Stanford University, Stanford, CA

Ph.D. in Electrical Engineering, 2002; M.S.E.E., 1993: Analog circuits, signal and image processing. Thesis: "Data Converters for High Speed CMOS Links", advisors Prof's. M. Horowitz and W. Dally Led design of 8 GSymbol/s multi-level transceiver based on 4-bit ADC and 8-bit DAC with equalization, digital phase recovery, and inductors to distribute parasitic input and output capacitance.

Rensselaer Polytechnic Institute, Troy, NY

B.S. in Electrical Engineering, 1983: Member, Eta Kappa Nu, Dean's list.

Professional Experience

President, Analog Circuit Works; Visiting Scientist, MIT; 2009-present

Founded company that designs integrated circuits for systems on chips (SoCs) in wireless, medical, computing and communications applications. Led design of IC for vision restoring prosthesis including wireless power and data, high voltage electrode drivers, ADC, safety monitoring.

Sr. Staff Engr, Qualcomm, 2006-2009

Leader of analog front end design team integrating ADCs, DACs, PLL, clocking and bias for femto-cell 45nm basestation IC, developed DAC performance enhancement techniques. Led design of gain-boosted pipeline ADC for 65nm multi-protocol wireless transceiver, functional 1st silicon. Ported band-switched LC PLL to 90nm, verified thoroughly, functional 1st silicon. Two patents, one pending.

Sr. Member Technical Staff, Maxim Integrated Products, 2004-2006

Led feasibility and PLL design for clock synthesizer product. Drove next-generation data converter project definition, designed circuit blocks. Characterized, simulated and modeled leading-edge A/D converters in basestation applications.

Lead Design Engineer, Analog Devices, 2001 to 2004

Design lead for 34 x 3 Gbit/s crosspoint switch with 4.5W power dissipation, 2 ps RMS phase noise, and process-independent linear and DFE equalization. Helped identify market opportunity, drove product requirements, defined architecture, designed receiver, equalizer, clock recovery, PLL circuits, datapath Verilog. Mentored designers in logic design and synthesis, clock distribution, GHz IC test, development of on-chip test sampling circuits. Designed and simulated 10 Gbit/s CMOS equalized transceiver. 2 patents issued, 1 pending.

Consultant, Transcendata, 1999

Researched architecture and circuits for a multi-level 10 Gbit/s optical transceiver.

Design Engineer, Manager; Raynet, 1987 to 1996

Designed high speed packet engine ASIC with rapid digital phase acquisition circuit. Created Makefile and Synopsys scripts for ASIC group. Wrote engineering portion of bid that won 20% of German fiber-to-the-home market. Awarded five patents, a Team Achievement and three Key Contributor awards.

Managed 7-member design group, defined and documented architecture for fiber-to-the-home headend electronics. Brought project in on schedule and under budget, meeting tough thermal and VDE Class B EMC requirements.

Integrated and debugged fiber-optic telephone distribution system, solved redundancy switching, jitter tolerance, and inrush current problems, wrote troubleshooting manual. Designed DS1 interface board, helped develop firmware. Led 9-man team in developing automated board test stations.

Engineer, M/A-COM 1986 to 1987

Designed DSP boards for jam-resistant satellite modem. Built shared memory with high-speed SRAM, reducing memory access time, cost and board space.

Design Engineer, Cybermation, 1983 to 1986; Summers 1979 to 1982

Co-inventor and principal designer of multi-axis motion controller, led four-man design team. Designed switching power amplifier for motor control. Developed real-time controller firmware, microcomputer operating system, C compiler and source debugger, error correcting communications protocol. Wrote software for a highly efficient irregular shape nester. Devised a general contour splitting program. Enhanced and debugged assembler language executive for motion controller.

Academic Projects

8 GSymbol/s multi-level transceiver

Led design of transceiver with 4-bit calibrated ADC and 8-bit DAC, phase interpolator clock recovery. Equalization algorithms and inductors to reduce parasitic losses compensate for the 1.5 GHz transceiver bandwidth to allow 8 GSample/s multi-level data transmission.

2 Gbit/s asymmetric transceivers

Led design of compact, robust transceivers for the Tiny Tera network switch. Asymmetric phase adjustment reduced the complexity and power of the crossbar chips. A test chip with integrating receiver and current-mode transmitter led to the design of a 50 MBit/s crossbar chip.

Selected Publications

Ellersick, W., “Real Portable Model for System/Verilog/A/AMS”, Synopsys User’s Group Conference, September 2010.

Ellersick, W., et al, “ADSX34: A 34 port, 3 Gbit/s, 4.5W Synchronous Crosspoint Switch”, Analog Devices General Technical Conference, April 2004.

Ellersick, W., et al, “3.2 Gbit/s Clock Recovery with LC PLL and Sinusoidal Phase Interpolators”, Analog Devices General Technical Conference, April 2002.

Ellersick, W., et al, "A Serial-Link Transceiver Based on 8-GSample/s A/D and D/A Converters in 0.25-µm CMOS". International Solid-State Circuits Conference, Feb. 2001, p. 58-59, author of subsequent Journal of Solid-State Circuits article, vol. 36, no. 11, Nov. 2001.

Ellersick, W., et al, "GAD: A 12-GS/s CMOS 4-bit A/D Converter for an Equalized Multi- Level Link". IEEE Symposium on VLSI Circuits, June 1999, p. 49-52.

McKeown, N., et al, "Tiny Tera: a packet switch core". IEEE Micro, Jan.-Feb. 1997. vol.17, no.1, p. 26-33 (Journal Paper).

Ellersick, W., "ASIC Design Tips for a Smooth Back End", Synopsys Users' Group Proceedings, San Jose, February 1996.

Ellersick, W., "Fault Detection and Isolation of Fiber to the Curb Systems", National Fiber Optic Engineering Conference, San Antonio, 1993.

Patents

7,692,468	Active Clamp to Protect Low-Voltage Devices in High-Voltage Circuits
In process	Low Power RF Divider
In process	Clock Recovery with Sinusoidal Phase Interpolators
7,499,489	CMOS 3 Gbit/s Receiver with Analog and Decision Feedback Equalization
7,427,866	Calibration and method for adjusting time constants of circuits
6,044,122	Digital Phase Acquisition with Delay Locked Loop
6,038,226	Combined Signalling and PCM Cross Connect and Packet Engine
5,801,867	DC-coupled receiver for shared optical system
5,402,479	Method and apparatus for translating signaling information
5,010,293	Inrush current limiting circuit
4,777,603	Controller for multiple-axis machine

Community Service

Coaching of youth soccer and ice hockey teams.